PUNJABI UNIVERSITY, PATIALA

REVISED SCHEME AND SYLLABI
FOR

MASTER OF TECHNOLOGY
(ELECTRONICS AND COMMUNICATION ENGG.)
REGULAR / PART TIME

(SEMESTER SYSTEM)
YEAR 2010-2011

LIST OF CORE COURSES

MEC-101 WIRELESS AND MOBILE DATA COMMUNICATION
MEC-102 OPTICAL COMMUNICATION SYSTEM
MEC-103 VLSI DESIGN
MEC-104 MICROCONTROLLERS AND EMBEDDED SYSTEMS
MEC-105 ADVANCED DIGITAL SIGNAL PROCESSING
MEC-106 RESEARCH METHODOLOGY

LIST OF ELECTIVE COURSES

MEC-201 ANTENNA SYSTEM ENGINEERING
MEC-202 DIGITAL IMAGE PROCESSING AND ANALYSIS
MEC-203 INFORMATION THEORY AND CODING
MEC-204 EMI AND EMC TECHNIQUES
MEC-205 SEMICONDUCTOR DEVICES AND MODELING
MEC-206 ARTIFICIAL NEURAL NETWORKS AND FUZZY SYSTEMS
MEC-207 MEMS AND MICROSYSTEMS TECHNOLOGY
MEC-208 TELECOMMUNICATION SWITCHING SYSTEMS AND NETWORKS
MEC-209 PROGRAMMABLE LOGIC CONTROLLER
MEC-210 NANOELECTRONICS DEVICES ENGINEERING
MEC-211 PARALLEL COMPUTING FUNDAMENTALS
MEC-212 SPEECH PROCESSING
MEC-213 COMPUTER SYSTEM ARCHITECTURE
MEC-214 MICROELECTRONICS TECHNOLOGY
MEC-215 ADVANCED DIGITAL SYSTEM DESIGN
MEC-216 ADVANCED MICROPROCESSORS AND INTERFACING
MEC-217 MULTIMEDIA COMPRESSION TECHNIQUES
MEC-218 MICROWAVE INTEGRATED CIRCUITS
MEC-219 GLOBAL TRACKING AND POSITIONING SYSTEMS
MEC-220 COMMUNICATION NETWORK SECURITY
MEC-221 RF SYSTEM DESIGN
MEC-222 DATA AND COMPUTER COMMUNICATION NETWORKS

SEMINAR AND MINOR PROJECT

MEC-301 ELECTRONICS ENGG. LAB
MEC302 SELF STUDY & SEMINAR
MEC-303 PROJECT

DISSERTATION

MEC-401 DISSERTATION

MEC-104 MICROCONTROLLERS AND EMBEDDED SYSTEMS

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3 1 0

Maximum Marks: 70 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40% **Lectures to be delivered: 45-55**

Instructions for paper-setter: The question paper will consist of five sections A, B, C, D and E. Sections A, B, C and D will have two questions from the respective sections of the syllabus. Section E will have one question with 10 short answer objective type parts, which will cover the entire syllabus uniformly. All questions will carry same marks.
Instructions for candidates: Candidates are required to attempt one question each from sections A, B, C and D of the question paper and the entire section E.

SECTION-A

Introduction: The Overview of 8051 Microcontroller Family, The Inside of 8051 Microcontroller, Pin Description of the 8051, Addressing Modes.

Instruction Set: Arithmetic, Logic and Single Bit Instructions, I/O instructions, etc.

SECTION-B

Assembly Language Programming: I/O Programming, Timer/Counter Programming, Serial communication, Interrupts Programming.

SECTION-C

Introduction to Embedded Systems: An Embedded System, Processor in the System, Hardware Units, Software, and Embedded System Examples.

Processor and Memory Organization: Structural Units in a Processor, Processor Selection for Embedded System, Memory Map, Interfacing Processor, Memories and I/O Devices.

SECTION-D

Devices and Buses: I/O Devices, Timer and Counting Devices, Serial and Parallel Communication Between Networked Multiple Devices Using I^2C, CAN, ISA, PCI and advanced I/O Buses.

Hardware-Software Co-design in an Embedded System: Embedded System Project Management, Design Issues in system Development Process, Design Cycle, Use of Target System and In-Circuit Emulator, Software tools for Development of Embedded System, Issues in Embedded System Design, Case Studies.

References:

1. Mazidi, "The 8051 Microcontroller and Embedded Systems, Pearson
2. Raj Kamal, "Embedded Systems," Tata McGraw Hill
3.Kenneth J. Ayala, "The 8051 Microcontroller," Penram International

MEC-105 ADVANCED DIGITAL SIGNAL PROCESSING

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3 1 0

Maximum Marks: 70 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40% **Lectures to be delivered: 45-55**

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SECTION-A

Introduction: Review of, classification of signals and systems, convolution, difference equations, correlation.

Fourier and Z Transforms: Properties of Fourier and Z transforms, Frequency analysis of discrete time signals and LTI Systems.

SECTION-B

Discrete Fourier Transform: Definition and properties of DFT, Linear filtering methods using DFT, Frequency analysis of signals using the DFT.

Fast Fourier Transform: FFT algorithms and their applications, linear filtering approach to computation of the DFT.

SECTION-C

Implementation of Discrete Time systems: Structure of IIR and FIR systems, state space analysis and structures, Quantization of filter co- efficients.

IIR Filter Design: IIR filter design by Impulse invariance, Bilinear Transformation, Matched-z Transformation and Approximation of Derivatives Methods Characteristics of commonly used Analog Filters.

FIR Filter Design: Symmetric & Antisymmetric FIR filter design by Frequency Sampling, Using windows methods.

SECTION-D

DSP Processors: Introduction to DSP Processors, Architecture TMS 320C54X and ADSP 2100 DSP processors.

Applications of DSP: Applications of DSP in Communications, speech processing, image processing, Biomedical and in Radars with case studies.

References:

1. *Johan G. Proakis and Dimitris G. Manolakis, "Digital Signal Processing Principles, Algorithms and Applications," PHI*
2. *N. G. Palan, "Digital Signal Processing," Tech Max Publications Pune*
3. *Nair, " Digital Signal Processing: Theory, Analysis and Digital Filter Design," PHI*
4. *Digital Signal Processing By Mitra*
5. *Oppenheim & Schafer, "Digital Signal Processing," PHI*

MEC- 213 COMPUTER SYSTEM ARCHITECTURE

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3- 1- 0

Maximum Marks: 70 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40% **Lectures to be delivered: 45-55**

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SECTION-A

Basic Computer Organization: Introduction, Organization & Architectural classification, Computer Evolution and Performance, computer System Buses, registers & stacks, ALU, CPU, Control Unit, Hardwired and Micro programmed Control.

SECTION-B

CPU Instruction Sets: Characteristics, Functions, Addressing modes and Formats, CPU Structure, Processor & Register Organization, RISC and Superscalar Processors, PowerPC, Pentium processors etc.
Computer Arithmetic: Integer & Floating Point Arithmetic.

SECTION-C

Memory and I/O Devices: Internal & External memory, Virtual & High-Speed memories, I/O Devices & Modules, Programmed & Interrupt driven I/O, DMA.

SECTION-D

Parallel Processing and Pipelining: Introduction, Parallelism in uniprocessor system, Memory interleaving, Pipelining and vector processing, Instructions and arithmetic pipelines, Array processor, parallel processing algorithms.

References:

1. John P. Hayes, "Computer Architecture and Organization", McGraw-Hill
2. Stallings, "Computer Organization and Architecture", Pearson Education
3. M. M. Mano, "Computer System Architecture", PHI
4. Patterson and Hennessy, "Computer Architectures", Morgaon Kauffman

MEC-220 COMMUNICATION NETWORK SECURITY

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Maximum Marks: 70 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40% **Lectures to be delivered: 45-55**

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Instructions for candidates: Candidates are required to attempt one question each from sections A, B, C and D of the question paper and the entire section E.

SECTION-A

CONVENTIONAL ENCRYPTION: Introduction, Conventional encryption model, Steganography, Data Encryption Standard, block cipher, Encryption algorithms, confidentiality, Key distribution.

PUBLIC KEY ENCRYPTION AND HASHING: Principles of public key cryptosystems, RSA algorithm, Diffie-Hellman Key Exchange, Elliptic curve cryptology, message authentification and Hash functions, Hash and Mac algorithms, Digital signatures.

SECTION-B

IP SECURITY: IP Security Overview, IP security Architecture, authentification Header, Security payload, security associations, Key Management.

SECTION-C

WEB SECURITY: Web security requirement, secure sockets layer, transport layer security, secure electronic transaction, dual signature.

SECTION-D

SECURITY SYSTEM: Intruders, Viruses, Worms, firewall design, Trusted systems, antivirus techniques, digital Immune systems.

References:

1. *William Stallings,"Cryptography and Network security", 2nd Edition ,Prentice Hall of India, New Delhi, 1999*
2. *Baldwin R and Rivest. R. "TheRC5,RC5-CBC,TC5-CBC-PAD and RC5-CT5 Algorithms,RFC2040",October1996.*

MEC- 222 DATA AND COMPUTER COMMUNICATION NETWORKS

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Maximum Marks: 70 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40% **Lectures to be delivered: 45-55**

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SECTION-A

Data Communication Techniques: Synchronous-Asynchronous Transmission, Digital Transmission, Transmission Media, Impairments, Data encoding Techniques

Communication Networks: Circuit switching, Message switching, Packet Switching. X.25, LAN Technologies, Virtual Circuits

Network Reference Models: OSI and TCP/IP, Layered architecture

SECTION - B

Data Link Layer: Design issue, framing, error control, flow control, HDLC, SDLC, data link layer in the Internet (SLIP, PPP)

Network Layer: Routing Algorithms, shortest path, distance vector routing, Link state routing, and multicast routing. Congestion control, traffic shaping, leaky bucket, token bucket, choke packets, load shedding, internetworking- connection oriented and connectionless, fragmentation, internet architecture and addressing, IP protocol, ICMP, APR, RARP, OSPF, BGP, CIDR, IPv6.

SECTION - C

Transport and Session Layer: Transport Service, quality of service, connection management, addressing, flow control and buffering, multiplexing, Internet transport protocols- TCP and UDP, Session layer- Dialogue management, synchronization and remote procedure call.

SECTION - D

Presentation Layer: date representation, data compression, network security and cryptography.
Application Layer: DNS, SNMP, Telnet, TFTP, NFS E- mail, SMTP and World Wide Web

References:

1. A. S. Tanenbaum, "Computer Networks", Pearson Education
2. W. Stallings," Data and Computer Communications", PHI
3. J.F. Kurose, K.W. Ross, "Computer Networking: A Top-Down Approach featuring the Internet", Pearson Education
4. L.L. Peterson, B.S. Davie, "Computer Networks: A Systems Approach", Pearson Education